Hi3536 H.265 Decoder Processor

Brief Data Sheet

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Hi3536 H.265 Decoder Processor

Key Specifications

Processor Core

ARM Cortex A17 quad-core@maximum 1.4 GHz
- 32 KB L1 I-cache, 32 KB L1 D-cache
- 1 MB L2 cache
- Main control processor for running peripheral drivers and applications

ARM Cortex A7 single-core@maximum 900 MHz
- 32 KB L1 I-cache, 32 KB L1 D-cache
- 128 KB L2 cache
- Video-related module control

Video Decoding Standards

H.265 Main Profile L5.1
H.264 Baseline/Main/High profile L5.0
- MPEG4 SP L0–3/ASP L0–5

MJPEG/JPEG baseline

Video Encoding Standards

H.264 Baseline/Main/High profile L5.1
MJPEG/JPEG baseline

Video Encoding/Decoding

H.265/H.264&JPEG encoding and decoding of multiple streams:
- 4-channel 4K x 2K (3840 x 2160)@30 fps H.265/H.264 decoding+2x1080p@30 fps H.264 encoding+4-channel 4K x 2K@2 fps JPEG encoding
- 16x1080p@30 fps H.265/H.264 decoding+2x1080p@30 fps H.264 encoding+16x1080p@2 fps JPEG encoding
- 9x1080p@30 fps H.265/H.264 decoding+4K x 2K@30 fps H.264 encoding+9x1080p@2 fps JPEG encoding
- 32x720p@30 fps H.265/H.264 decoding+4x720p@30 fps H.264 encoding+32x720p@2 fps JPEG encoding
- 64xD1@30 fps H.265/H.264 decoding+8xD1@30 fps H.264 encoding+64xD1@2 fps JPEG encoding
- 9x720p@30 fps JPEG decoding

CBR or VBR, ranging from 16 kbit/s to 40 Mbit/s
Encoding frame rate ranging from 1 fps to 60 fps
ROI encoding
Color-to-gray encoding

GPU

Integrated Mali-T720 GPU
- OpenGL ES3.1/2.0/1.1
- OpenCL 1.2/1.1/1.0

Up to 63 MTris/s triangle filling rate
Double-precision FP64 and anti-aliasing

Intelligent Video Analysis

Integrated IVE 2.0, supporting various intelligent analysis applications:
- Motion detection
- Video diagnosis
- Perimeter protection

Video and Graphic Processing

3D denoising, deinterlacing, edge smoothing, dynamic contrast enhancement and sharpening
Anti-flicker for output videos and graphics
1/8x to 16x video scaling
1/2x to 2x graphic scaling
Four cover regions
OSD overlaying of eight regions

Video Interfaces

VI interfaces
- One BT.1120 HD input port
- One video input channel for dual-chip cascading
- SDR and DDR modes
- Maximum input of 1080p@60 fps in SDR mode
- Maximum input of 3840 x 2160@30 fps in DDR mode

VO interfaces
- One HDMI 2.0 ultra-HD output interface, support output up to 3840 x 2160@60 fps
- One VGA HD output interface, support output up to 2560 x 1600@60 fps
- One BT.1120 HD output port, supporting the maximum output of 1080p@60 fps in SDR mode or 3840 x 2160@30 fps in DDR mode
- Two independent HD output channels (DHD0 and DHD1), output from any HD interface (HDMI, VGA, and BT.1120)
- 64-picture output for DHD0, maximum 3840 x 2160@60 fps output
- 32-picture output for DHD1, maximum 1080p@60 fps output
- One CVBS SD output interface
- Three full-screen GUI graphics layers in RGB1555 or RGB8888 format, used by two HD channels and one SD channel
- Two hardware cursor layers in RGB1555, RGB4444 or RGB8888 format, with the maximum resolution of 256 x 256

Audio Interfaces

One integrated audio CODEC
Three unidirectional I^2S/PCM interfaces
- One input, supporting 16 multiplexed inputs
- Two outputs

16-bit audio input and output

Ethernet Ports

Two gigabit Ethernet ports
- RGMII, RMII, and MII modes
- 10/100 Mbit/s full-duplex or half-duplex
- 1000 Mbit/s full-duplex
- TOE for reducing the CPU usage

Security Engine

AES, DES, 3DES algorithms

HASH abstract algorithm

RAID Acceleration Engine

XOR acceleration
Up to nine data sources for XOR
DMA, up to 16 MB data block
Memory initialization (configurable initial value)
Descriptor linked list

Peripheral Interfaces

Two SATA 3.0 interfaces
- PM
- eSATA

One PCIe 2.0/SATA 3.0 interfaces
- Two PCIe interfaces, one PCIe interface+one SATA interface, or two SATA interfaces
- RC and EP supported as the PCIe 2.0 interface
- eSATA supported as the SATA 3.0 interface

Two USB 2.0 host ports, supporting hub
One USB 3.0 host port, supporting hub
Two SDIO interfaces
- SD 2.0, SDIO 2.0, MMC 4.4.1, and SDXC (only 3.3 V mode) cards supported for SDIO0 and SDIO1
- Only eMMC 4.5 card supported for SDIO1
- Multiplexing between SDIO0 and BT.1120 output pins
- Multiplexing between SDIO1 and NAND flash interface pins

Four UART interfaces, two of which supporting four wires
One IR interface
One I^2C interface
Multiple GPIO interfaces
One low-speed ADC interface

Memory Interfaces

Two 32-bit DDR3/4 SDRAM interfaces
- Maximum frequency of 933 MHz (1.866 Gbit/s)
- Dual channels
- ODT
- Maximum capacity of 3 GB

SPI NOR/NAND flash interface
- 1-/2-/4-bit SPI NOR/NAND flash
- Two CSs
- Maximum 32 MB for each CS (for only the NOR flash)
- Maximum 8 GB for each CS (for only the NAND flash)
- 2 KB/4 KB page size (for only the NAND flash)
- 8-bit/1 KB and 24-bit/1 KB ECC (for only the NAND flash)

NAND flash interface
- 8-bit NAND flash
- Two CSs
- SLC or MLC
- 8-/24-/40-/64-bit ECC based on the 1 KB data block

Embedded 64 KB BOOTROM and 88 KB SRAM

RTC with an Independent Power Supply

Independent battery for supplying power to the RTC

Boot Modes

Booting from the BOOTROM
Booting from the SPI NOR flash
Booting from the SPI NAND flash
Booting from the NAND flash
Booting from the eMMC
Booting the slave chip over the PCIe interface

SDK

Linux 3.10-based SDK
Audio encoding and decoding libraries complying with various protocols
High-performance H.265/H.264 PC decoding library

Physical Specifications

Power consumption
- Typical power consumption of 4.3 W
- Multi-level power-saving control

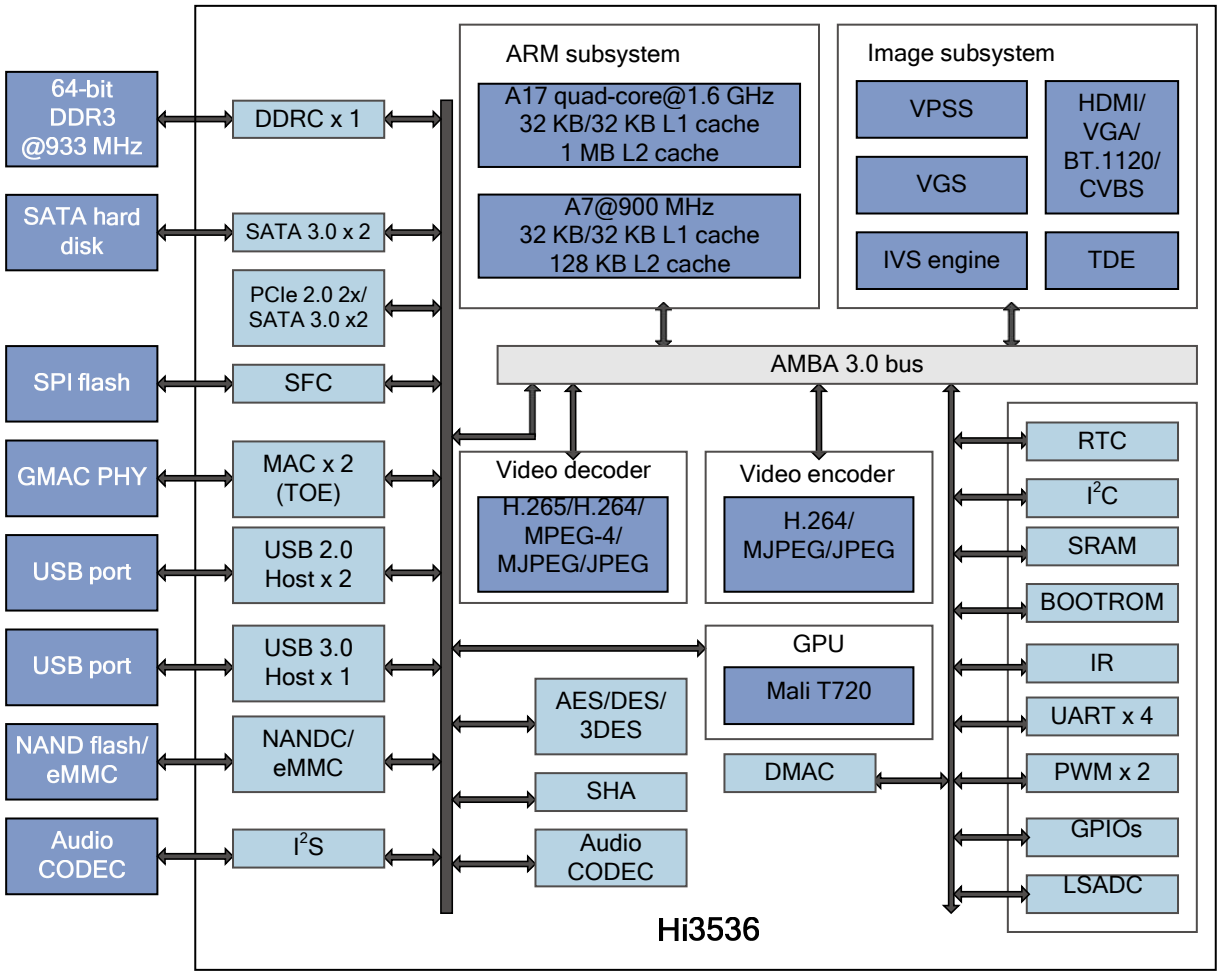
Operating voltages
- 0.9 V core voltage
- 1.0 V CPU voltage (or decreased to 0.9 V)
- 3.3 V I/O voltage
- 1.5/1.2 V DDR3/4 SDRAM interface voltage

Package
- RoHS, EDHS-PBGA
- Ball pitch of 0.8 mm (0.02 in.)
- Body size of 27 mm x 27 mm (1.06 in. x 1.06 in.)

- Operating temperature ranging from 0°C (32°F) to 70°C (158°F)

Hi3536 H.265 Decoder Processor

Functional Block Diagram



The Hi3536 is a professional high-end SoC targeted for the multi-channel HD or D1 NVR. The Hi3536 provides a high-performance A 17 processor, a video decoding engine (a maximum of 16x1080p decoding complying with various protocols), a high-performance video/graphics processing engine (various complicated graphics processing algorithms), and dual-channel HD outputs. These features enable the Hi3536 to provide high-quality images. In addition, the Hi3536 integrates various peripheral interfaces to meet differentiated customer requirements for functionality, features, and image quality, while reducing the eBOM cost.

NVRs (Each with a Hi3536)

16x1080p NVR

32x1080p@10 Mbit/s streams
16x1080p real-time decoding (16-channel polling previewing)
2x1080p real-time encoding
1080p@32 fps JPEG snapshot
HDMI 4K x 2K@30 fps 16-picture ultra-HD output

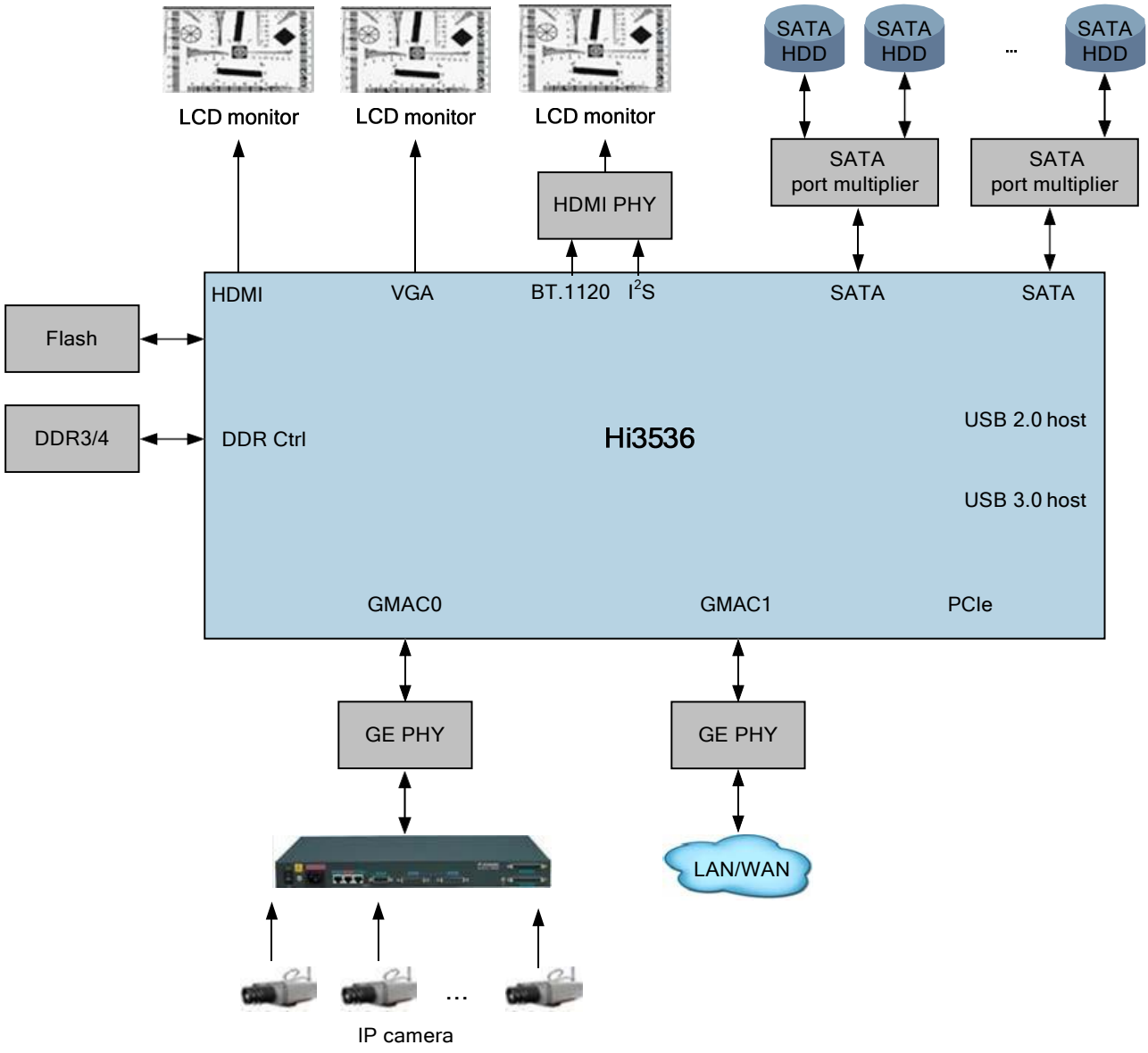
32x720p NVR

64x720p@5 Mbit/s streams
32x720p real-time decoding (32-channel polling previewing)
4x720p real-time encoding

720p@64 fps JPEG snapshot
HDMI+VGA 1080p@60 fps HD dual 16-picture output

64xD1 NVR

128xD1@2.5 Mbit/s streams
64xD1 real-time decoding (64-channel real-time previewing)
8xD1 real-time encoding
D1@128 fps JPEG snapshot
HDMI 4K x 2K@30 fps 64-picture ultra-HD output



Acronyms and Abbreviations

3DES	triple data encryption standard
AES	advanced encryption standard
CBR	constant bit rate
CS	chip select
CVBS	composite video broadcast signal
DDR	double-data rate
DES	data encryption standard
DMA	direct memory access
ECC	error correcting code
EP	endpoint
eSATA	external serial advanced technology attachment
GPIO	general-purpose input/output
GUI	graphical user interface
HD	high-definition
HDMI	high-definition multimedia interface
I^2C	inter-integrated circuit
I^2S	inter-IC sound
IR	infrared
IVE	intelligent video engine
MII	media independent interface
MLC	multi-level cell
NVR	network video recorder
ODT	on-die termination
OSD	on-screen display
PBGA	plastic ball grid array
PCIe	peripheral component interconnect express
PM	port multiplexer
RAID	redundant array of independent disks
RC	root complex
RGMII	reduced gigabit media independent interface
RMII	reduced media independent interface
RoHS	restriction of the use of certain hazardous substances
ROI	region of interest
RTC	real-time clock
SATA	serial advanced technology attachment
SD	standard-definition
SDR	single data rate
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SHA	secure hash algorithm
SLC	single-level cell
SMMU	system memory management unit
SoC	system-on-chip
SP	simple profile
SPI	serial peripheral interface
SRAM	static random access memory
TOE	TCP/IP offload engine
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VGA	video graphics array
VO	video output